

Memory Dependence Checking

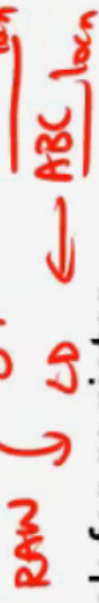
Mem

Ld R _k	0x abcdef
Ld	
St	abcd00
Ld	
Ld R _k	0x abcdef
St R _s	0x abcd00
Ld	0x abc000
Ld R _k	0x abcd00



- The issue queue checks for register dependences and executes instructions as soon as registers are ready

- Loads/stores access memory as well - must check for RAW, WAW, and WAR hazards for memory as well



- Hence, first check for register dependences to compute effective addresses; then check for memory dependences

possible RAW Mem