# Additional Details

- When does the decode stage stall? When we either run out of registers, or ROB entries, or issue queue entries

4 → Peak IPC = 4 → Avg IPC = 1–1.5

- Issue width: the number of instructions handled by each stage in a cycle. High issue width → high peak ILP

3 Peak IPC = 3 → Avg IPC = 0.8 → 1.2

- Window size: the number of in-flight instructions in the pipeline. Large window size → high ILP

ROB 40 → 60 Avg IPC : 1.0 → 1.2

- No more WAR and WAW hazards because of rename registers – must only worry about RAW hazards