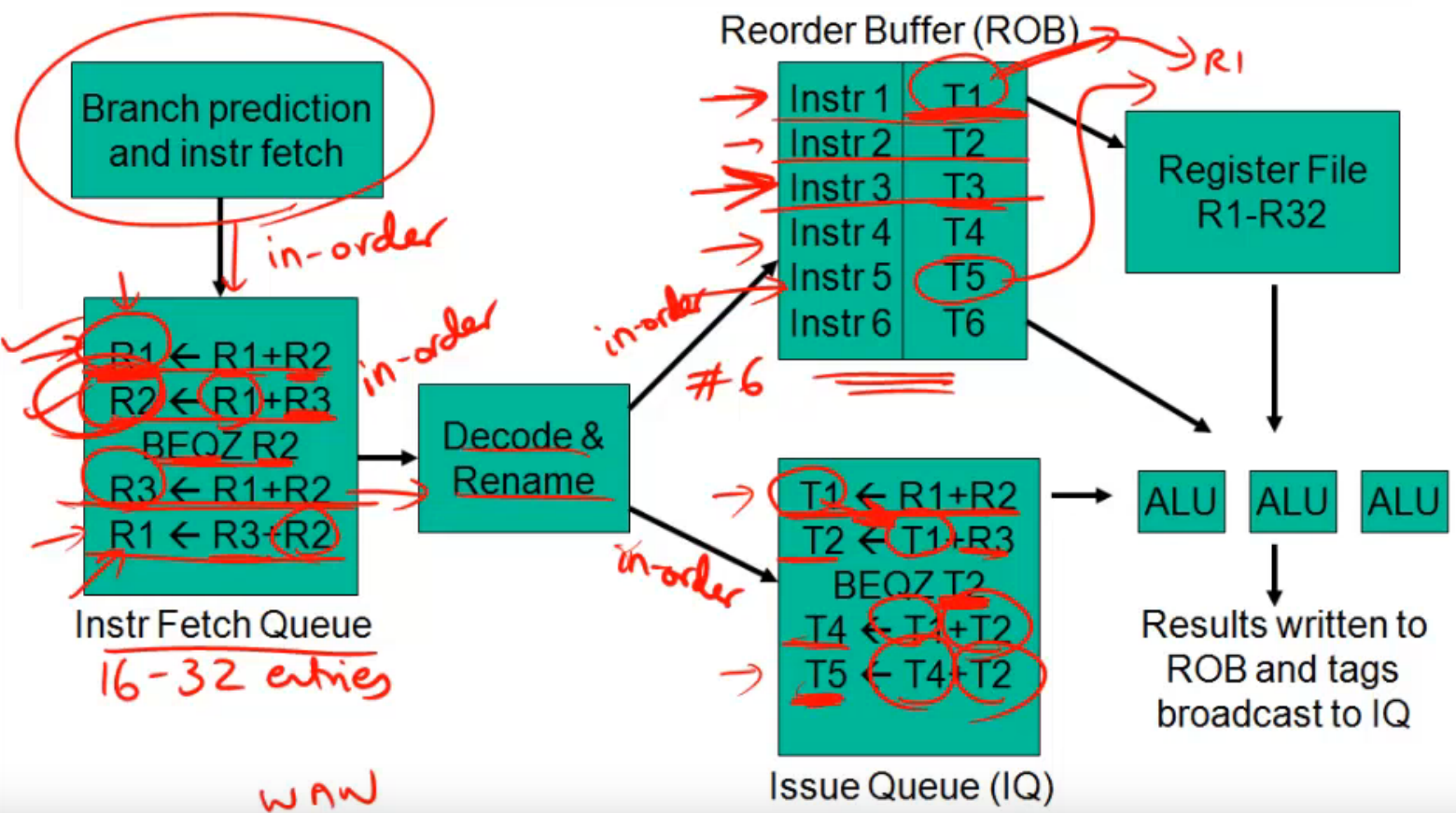
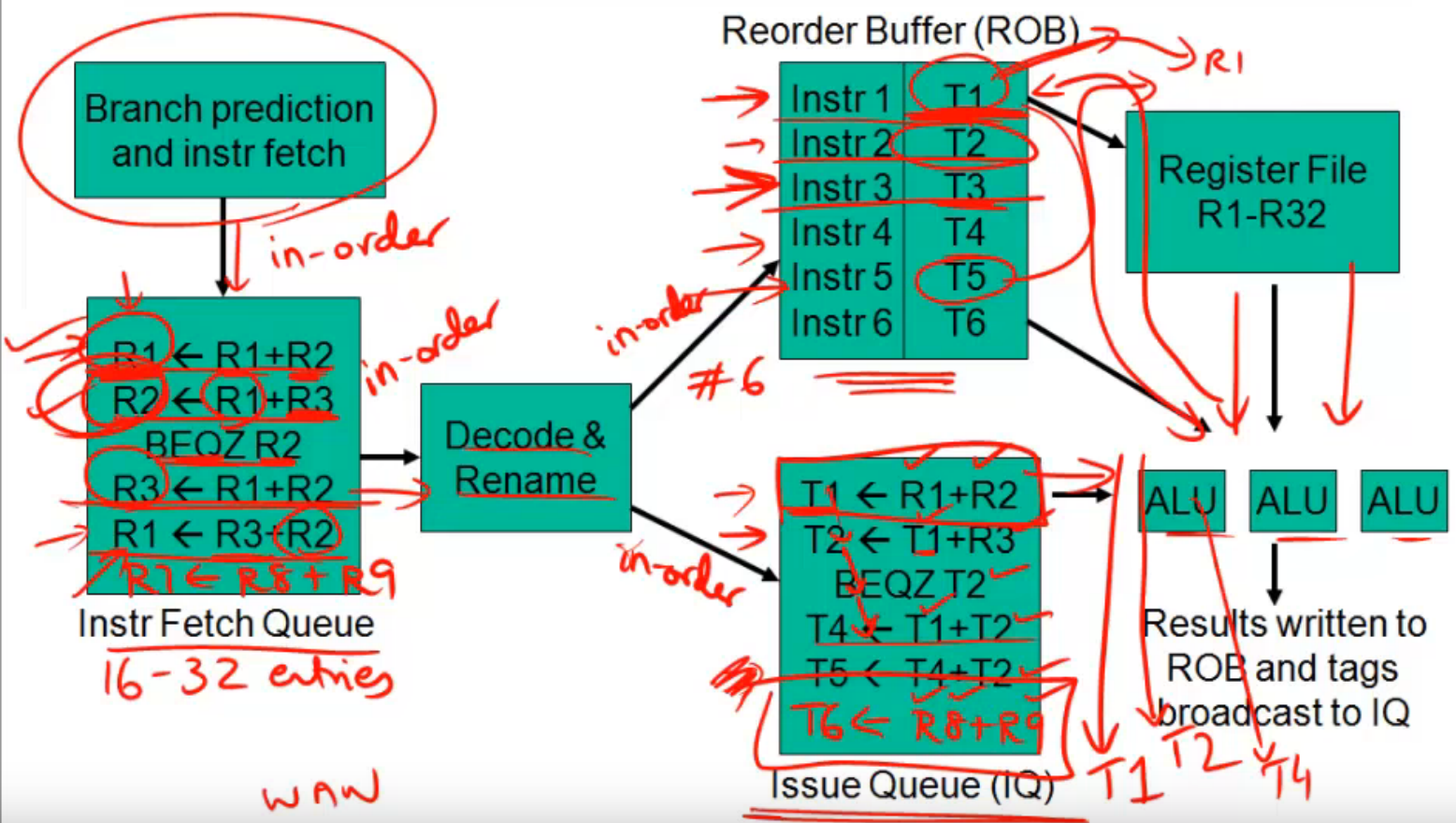


An Out-of-Order Processor Implementation



An Out-of-Order Processor Implementation



An Out-of-Order Processor Implementation

Branch prediction and instr fetch

in-order

~~$R1 \leftarrow R1 + R2$~~
 ~~$R2 \leftarrow R1 + R3$~~
~~BEQZ R2~~
 ~~$R3 \leftarrow R1 + R2$~~
 ~~$R1 \leftarrow R3 + R2$~~
 ~~$R7 \leftarrow R8 + R9$~~

Instr Fetch Queue

16-32 entries
 $\leftarrow R7 + R8$
WAW

Decode & Rename

in-order

~~$T1 \leftarrow R1 + R2$~~
 ~~$T2 \leftarrow T1 + R3$~~
~~BEQZ T2~~
 ~~$T4 \leftarrow T1 + T2$~~
 ~~$T5 \leftarrow T4 + T2$~~
 ~~$T6 \leftarrow R8 + R9$~~

Issue Queue (IQ)

$\leftarrow T6$

Reorder Buffer (ROB)

| | |
|---------|----|
| Instr 1 | T1 |
| Instr 2 | T2 |
| Instr 3 | T3 |
| Instr 4 | T4 |
| Instr 5 | T5 |
| Instr 6 | T6 |

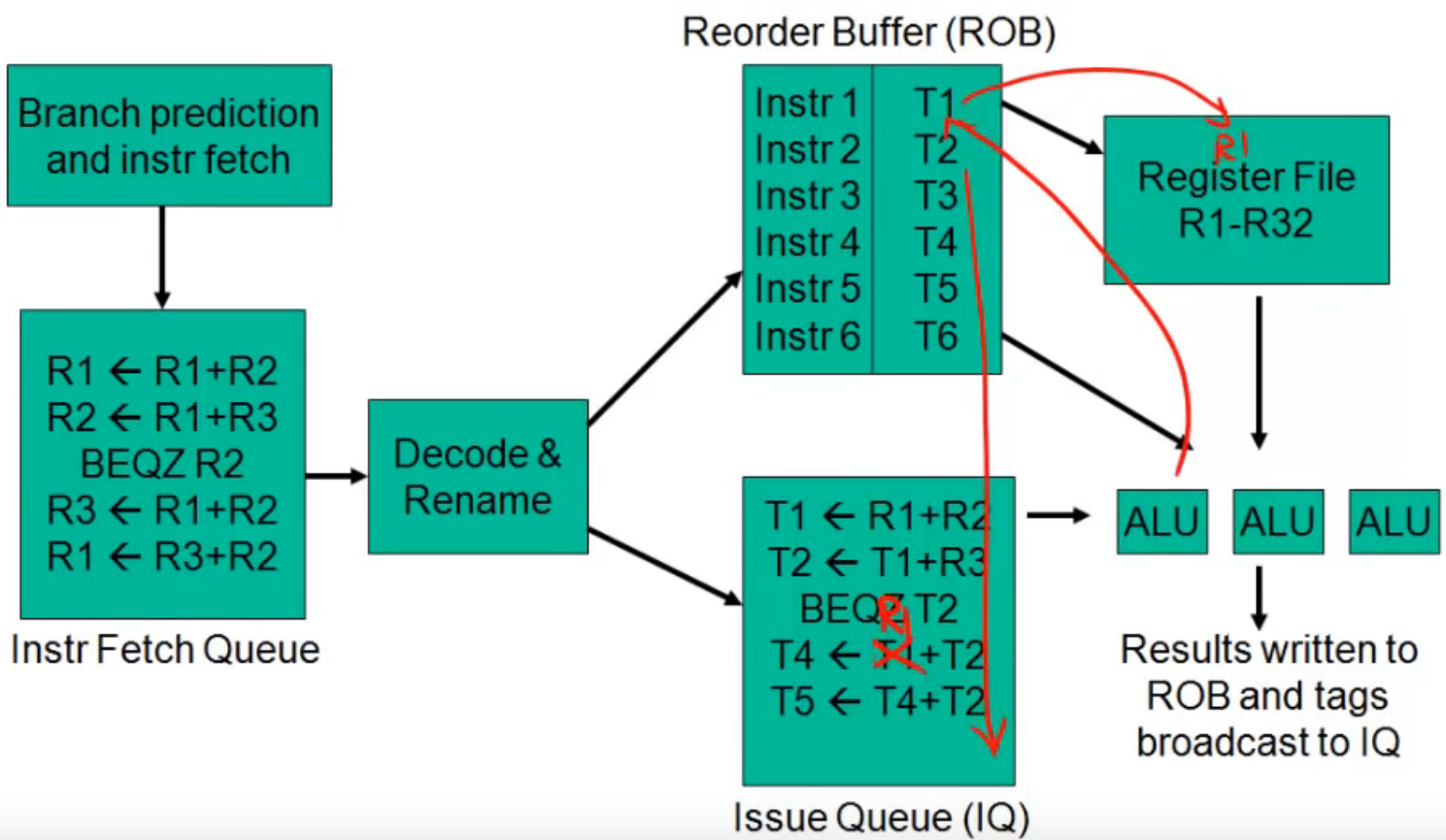
Register File
R1-R32

ALU ALU ALU

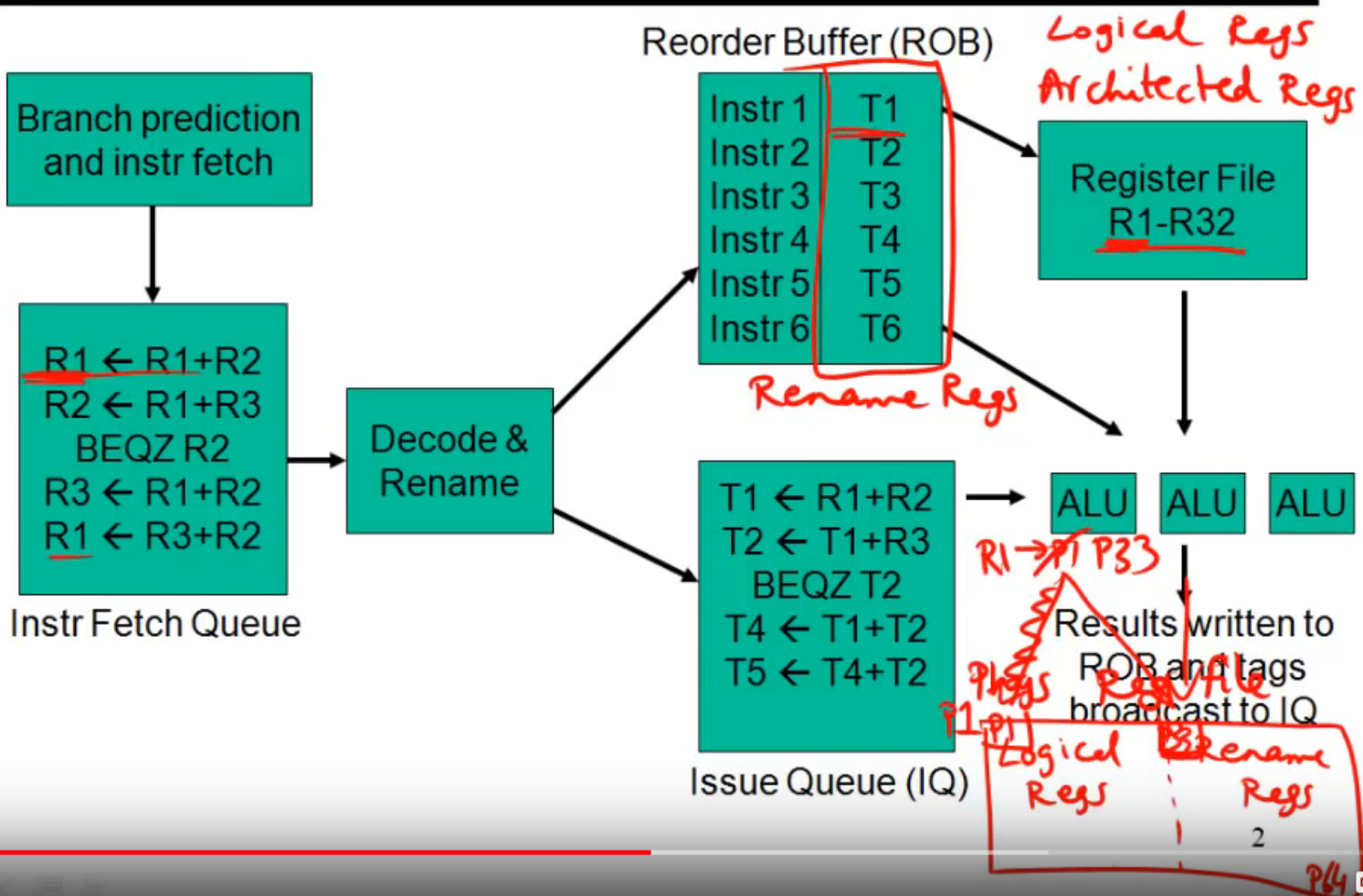
Results written to ROB and tags broadcast to IQ

$T1 T2 T4$

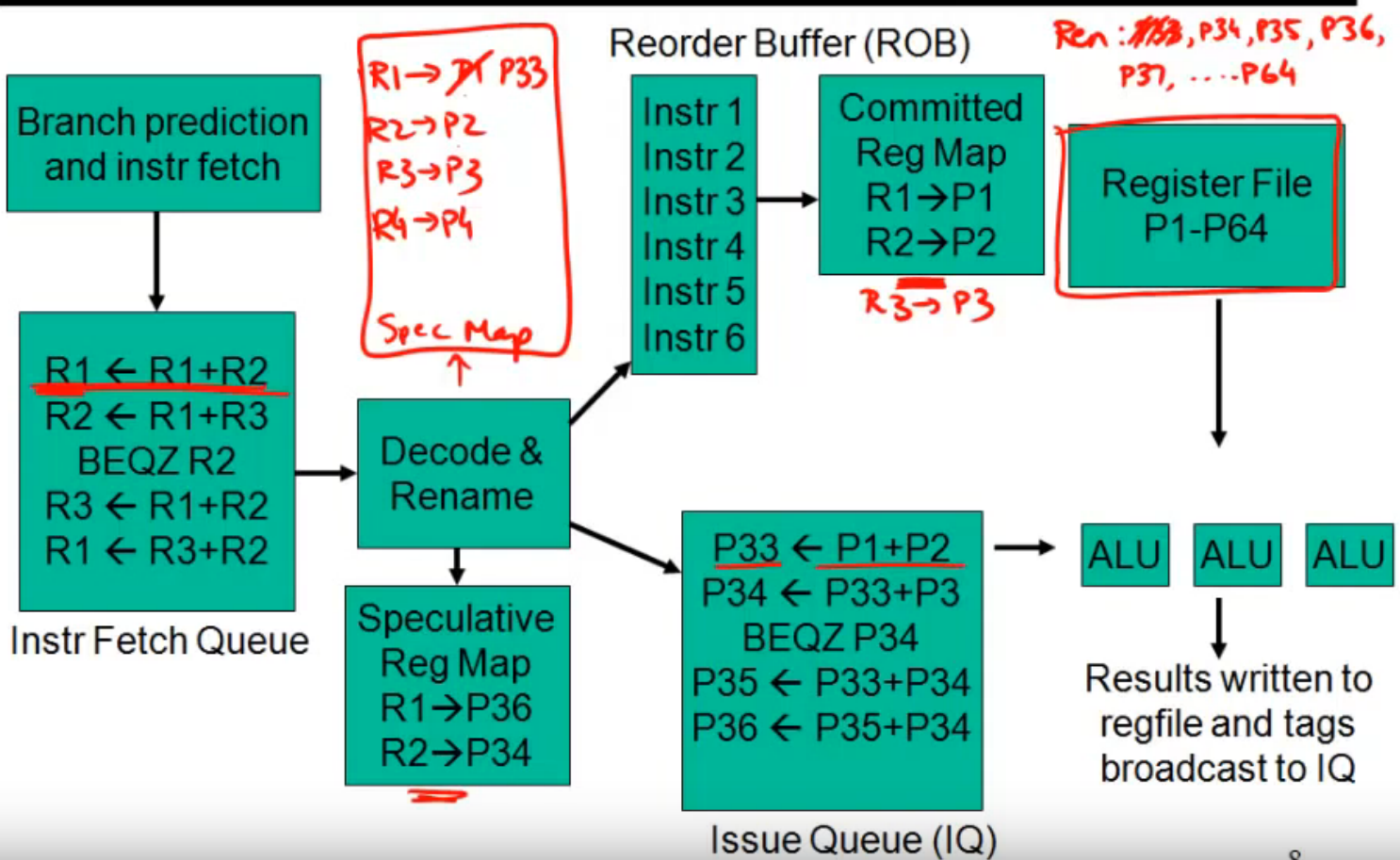
An Out-of-Order Processor Implementation



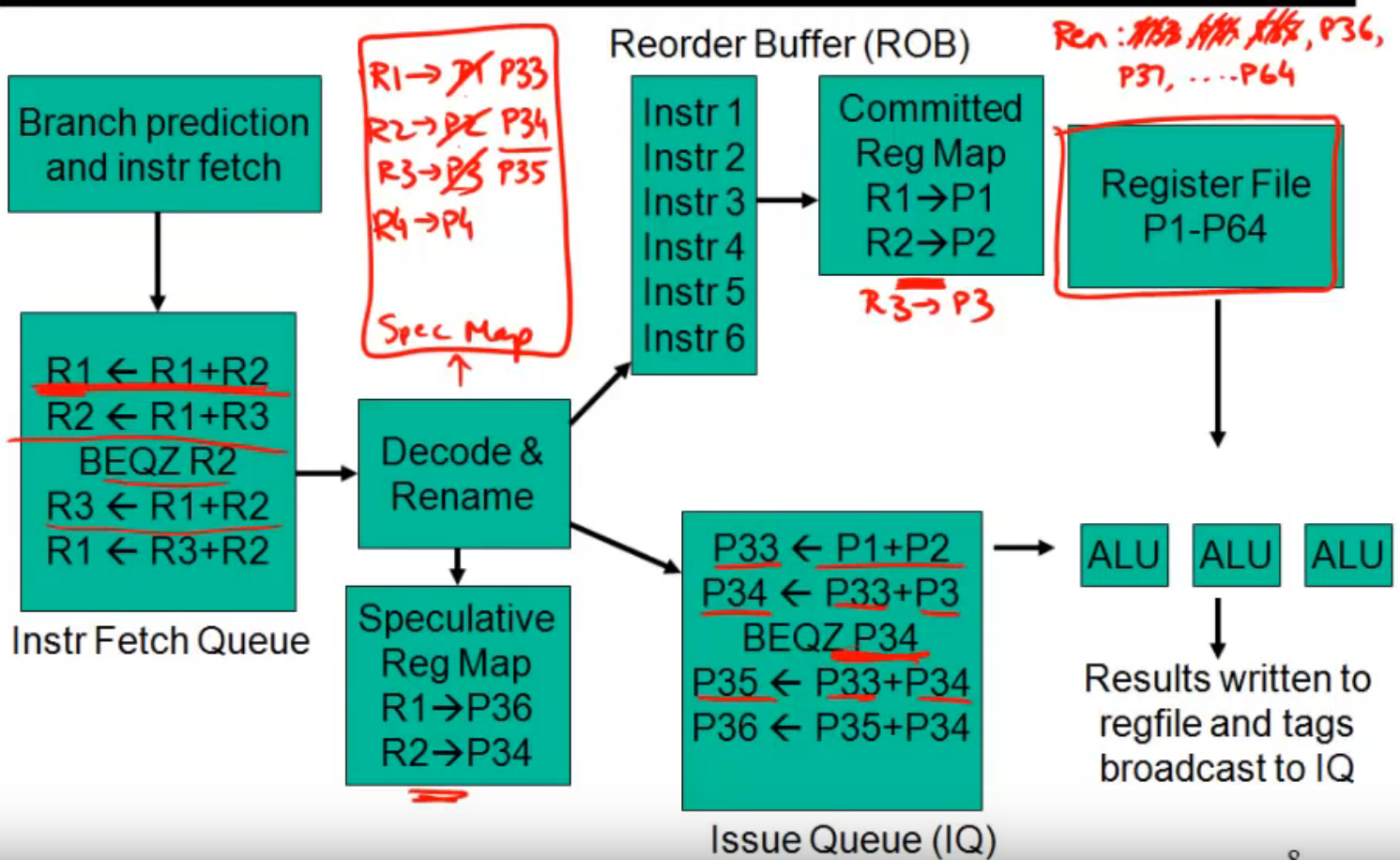
An Out-of-Order Processor Implementation



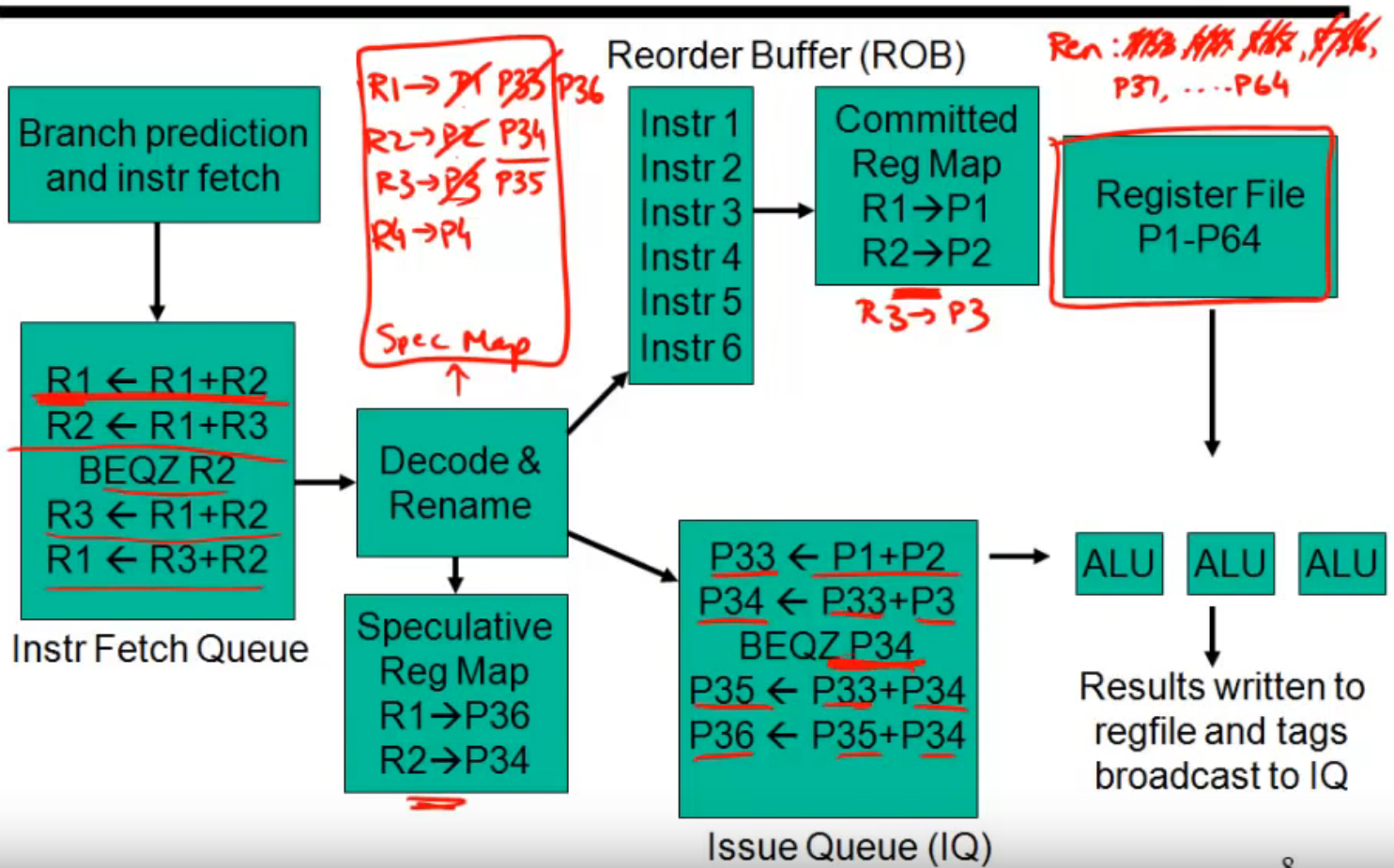
The Alpha 21264 Out-of-Order Implementation



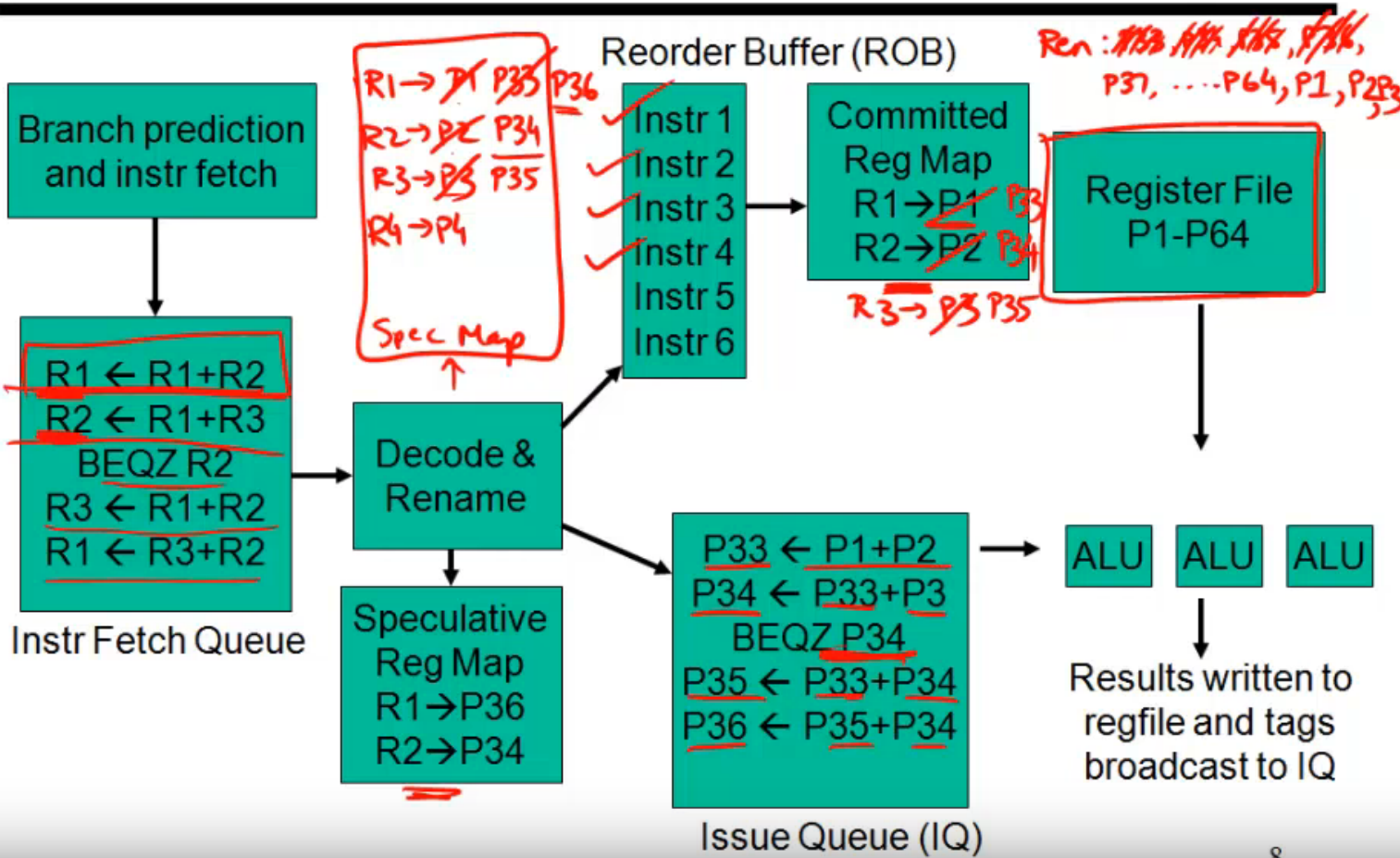
The Alpha 21264 Out-of-Order Implementation



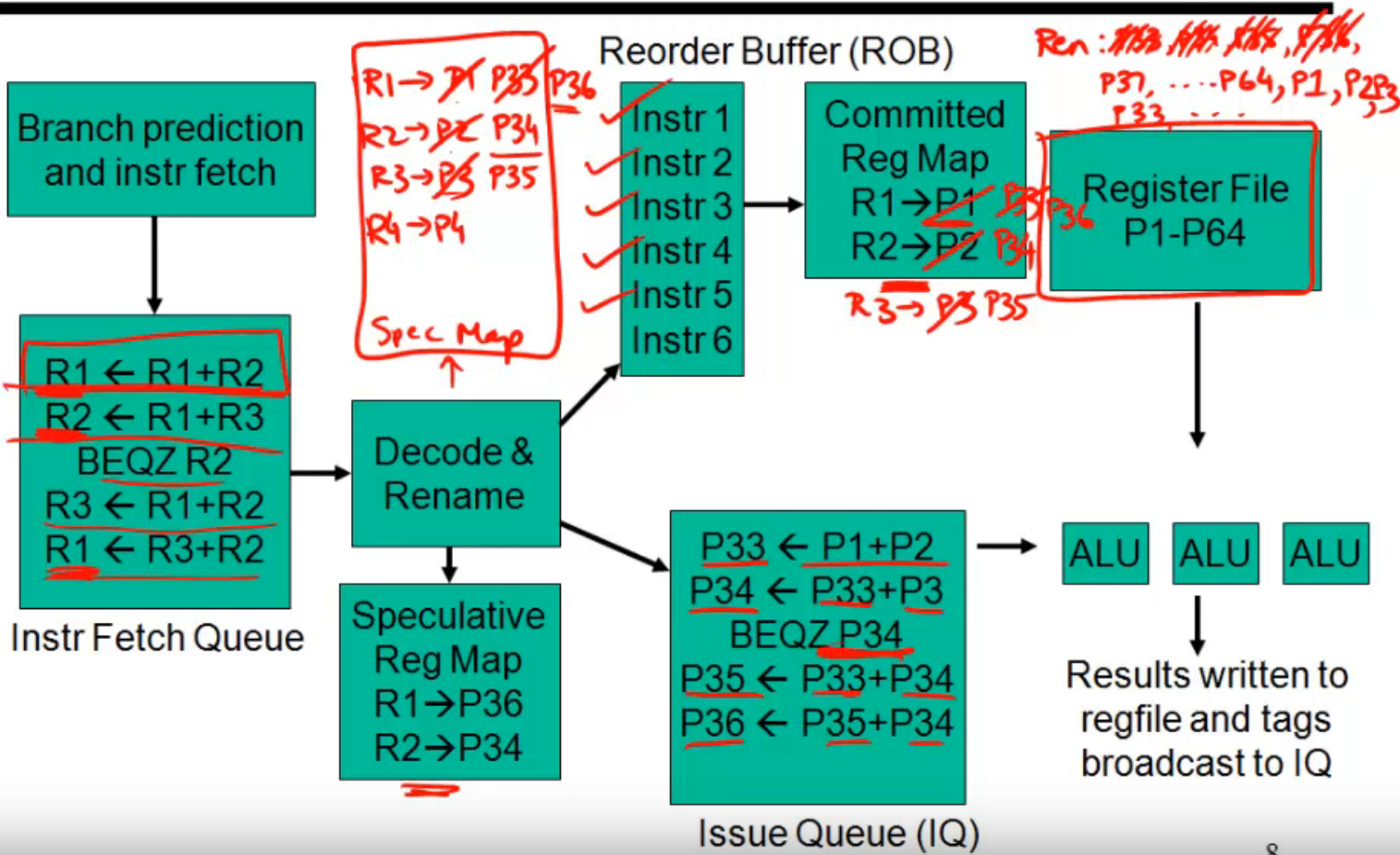
The Alpha 21264 Out-of-Order Implementation



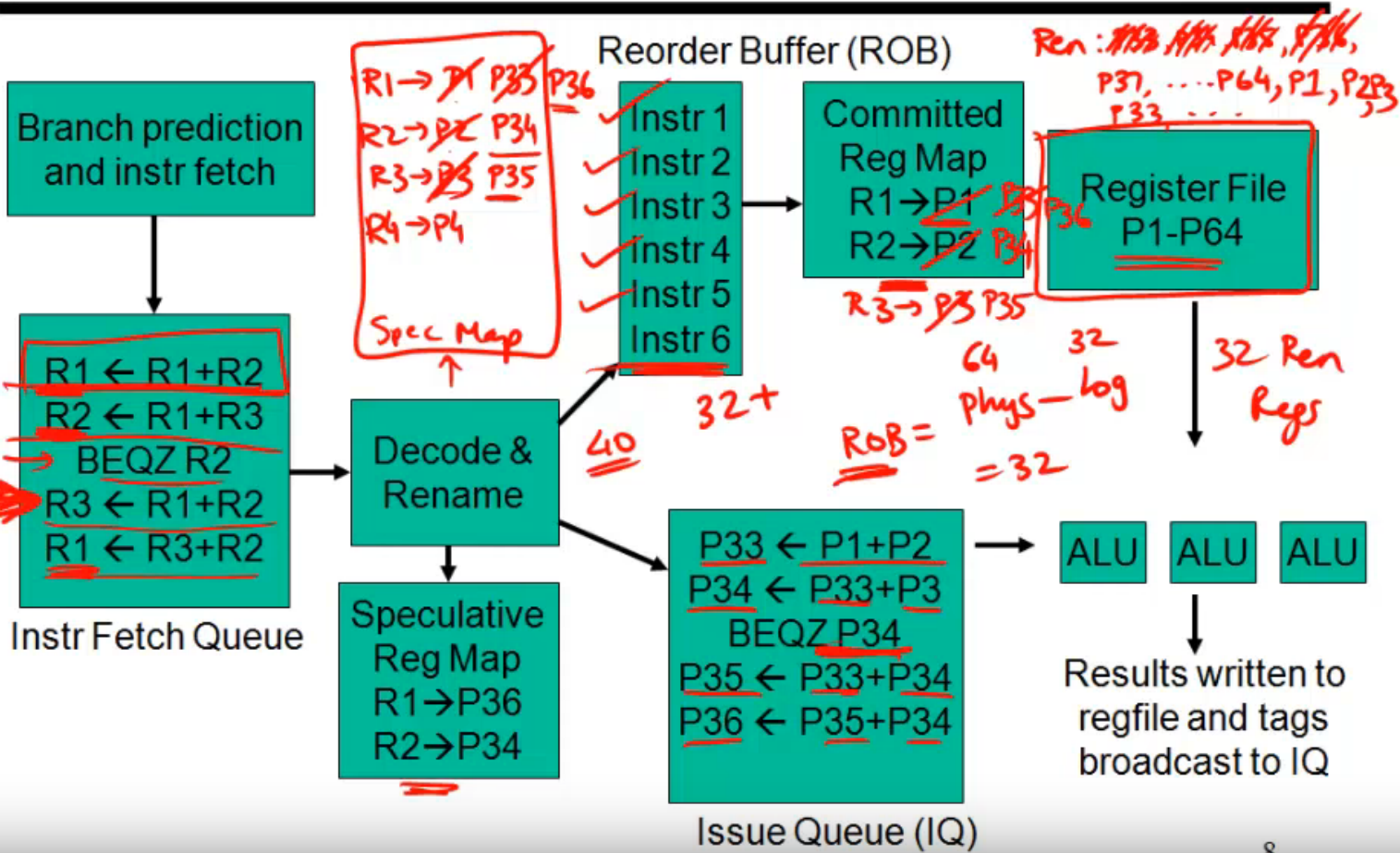
The Alpha 21264 Out-of-Order Implementation



The Alpha 21264 Out-of-Order Implementation



The Alpha 21264 Out-of-Order Implementation



The Alpha 21264 Out-of-Order Implementation

