Impact of Cache Coherence Protocols on the Power Consumption of STT-RAM-Based LLC

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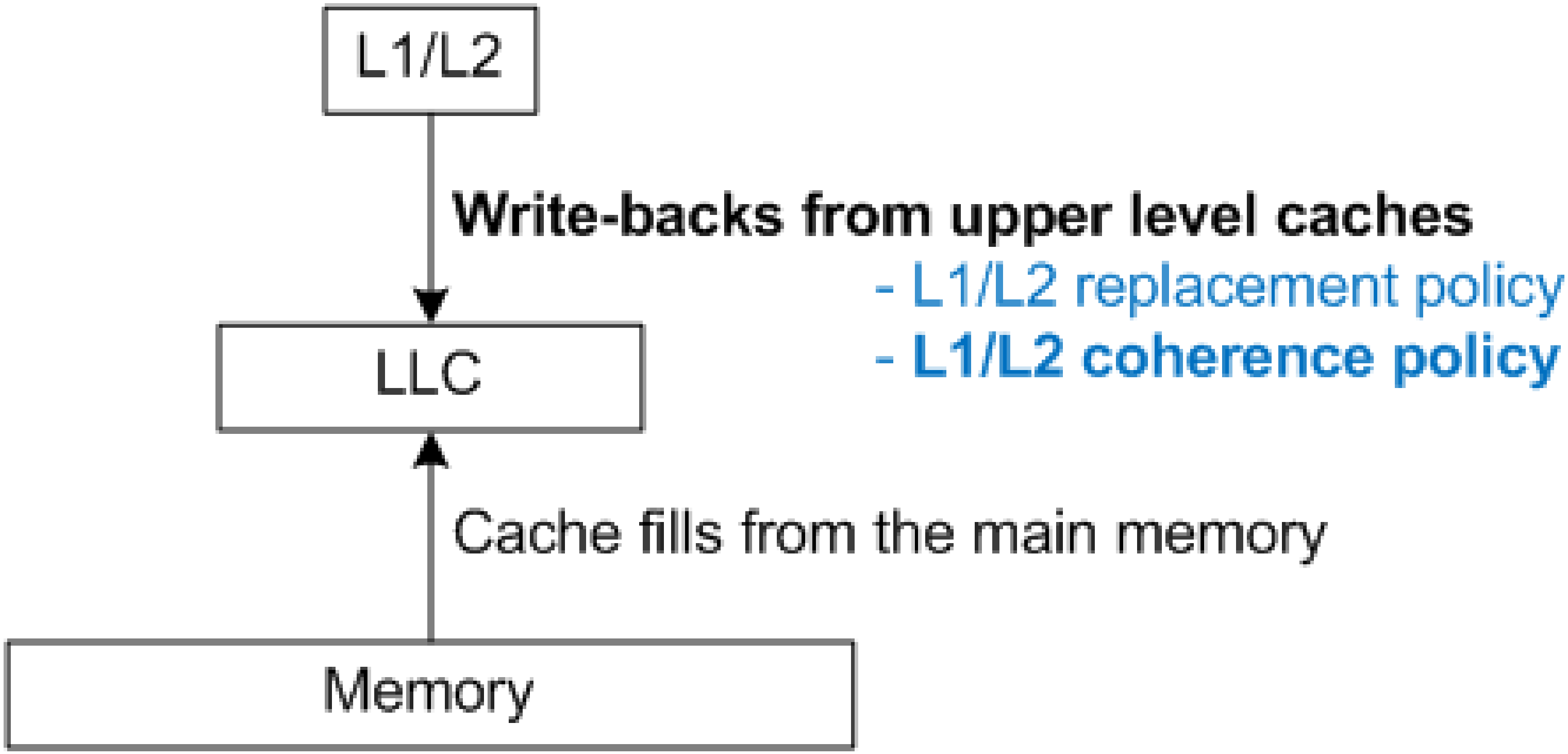
STT-RAM

- **A type of magnetic RAM**
  - **Storage = MTJ (Magnetic Tunneling Junction)**
- **An alternative to SRAM**

	(+)	(-)
SRAM	Fast	Large area Leakage
STT-RAM	Non-volatile Potential to scale	Extra process Long write time High write energy

Sources of LLC Writes



Motivation

- **STT-RAM requires high write energy**
- **Cache coherence protocol affects #write-backs and #broadcasts**
- **This work: the impact of cache coherence protocols on STT-RAM LLC power**

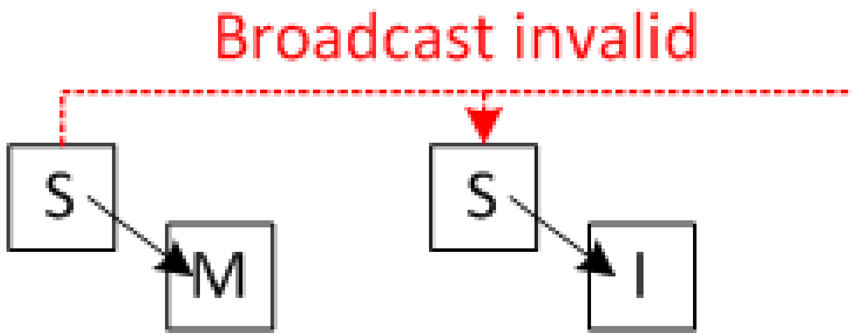
Cache Coherence Protocols

- **MSI: Modified, Shared, Invalid**
- **MESI: add Exclusive**
- **MOSI: add Owned**
- **MOESI: add Owned and Exclusive**

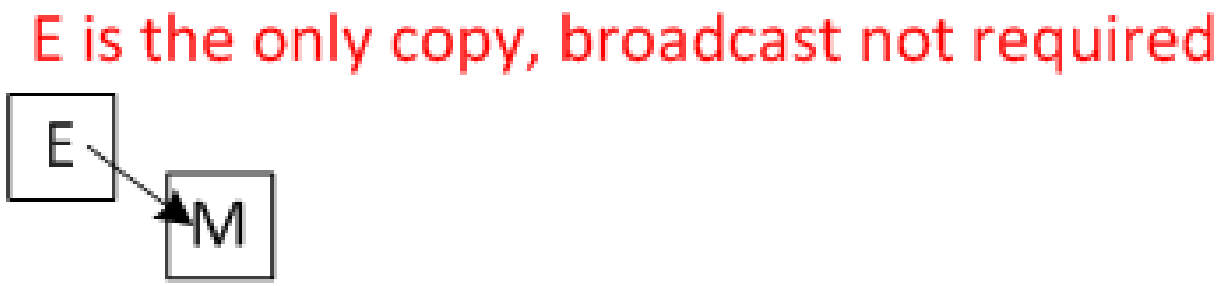
MESI vs. MSI

On write

MSI

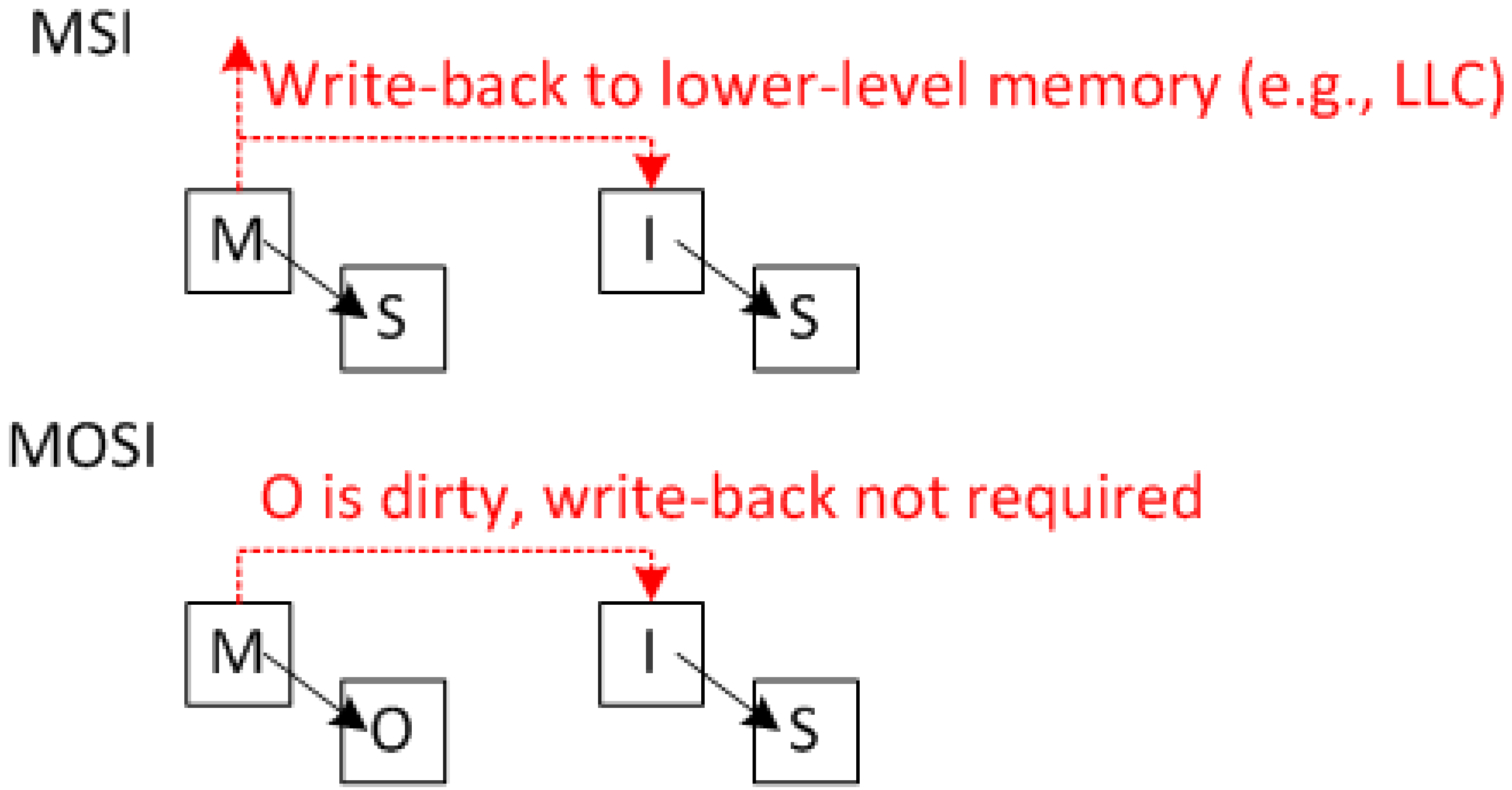


MESI



MOSI vs. MSI

On remote read hit



Cache Coherence Protocols

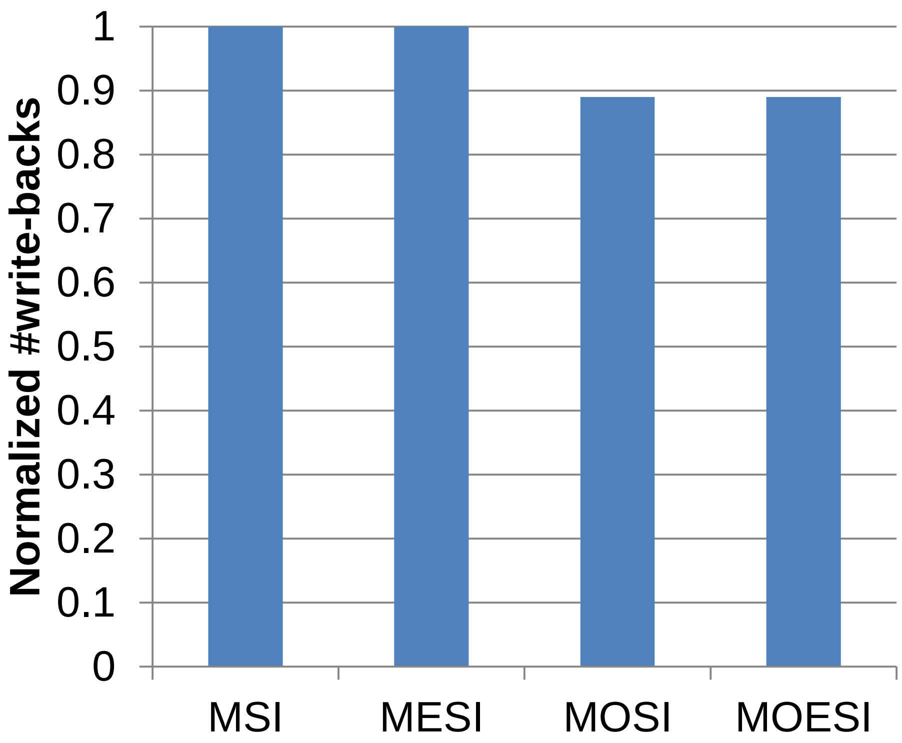
MSI	Low complexity
MESI	Reduce #broadcasts; medium complexity
MOSI	Reduce #write-backs; medium complexity
MOESI	Reduce #broadcasts and #write-backs; high complexity

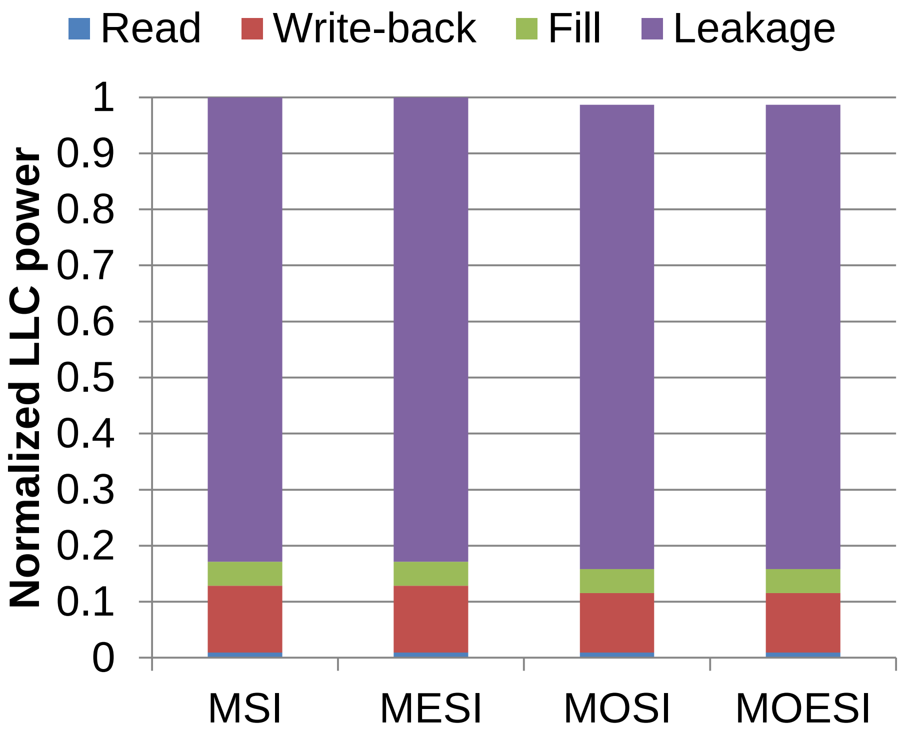
Methodology

- Full-system simulation
  - Modified MARSS
  - Snoopy-based MSI, MESI, MOSI, MOESI
- Cache and bus power/performance modeling
  - Modified CACTI
  - Bus model [Ghoniema et al. TCAS-I 2009]
- PARSEC benchmarks
  - 8 workloads; 3 input sets

Processor	8-core Atom, 2GHz
L1I (SRAM)	Private 32KB per core, 8-way, 64B
L1D (SRAM)	Private 32KB per core, 8-way, 64B
LLC (STT-RAM)	Shared 16MB write-back cache, 16-ways, 64B

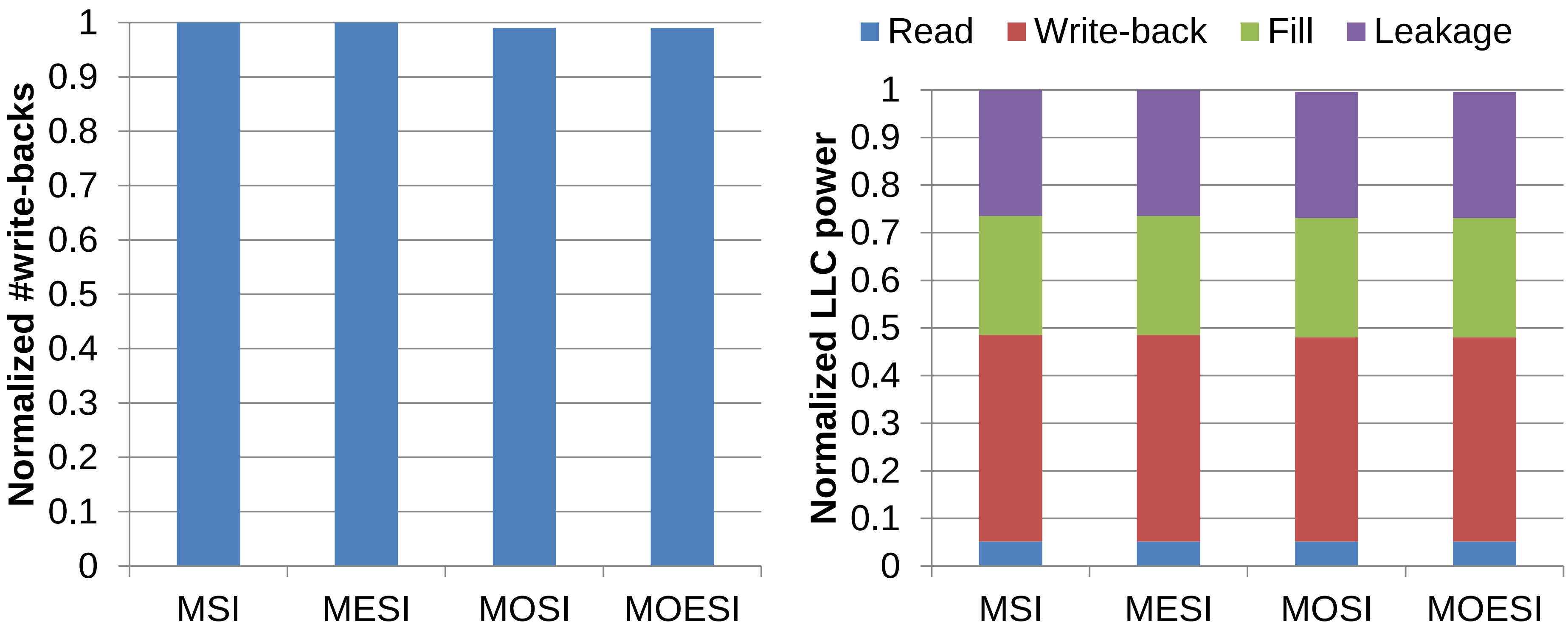
STT-RAM LLC Power





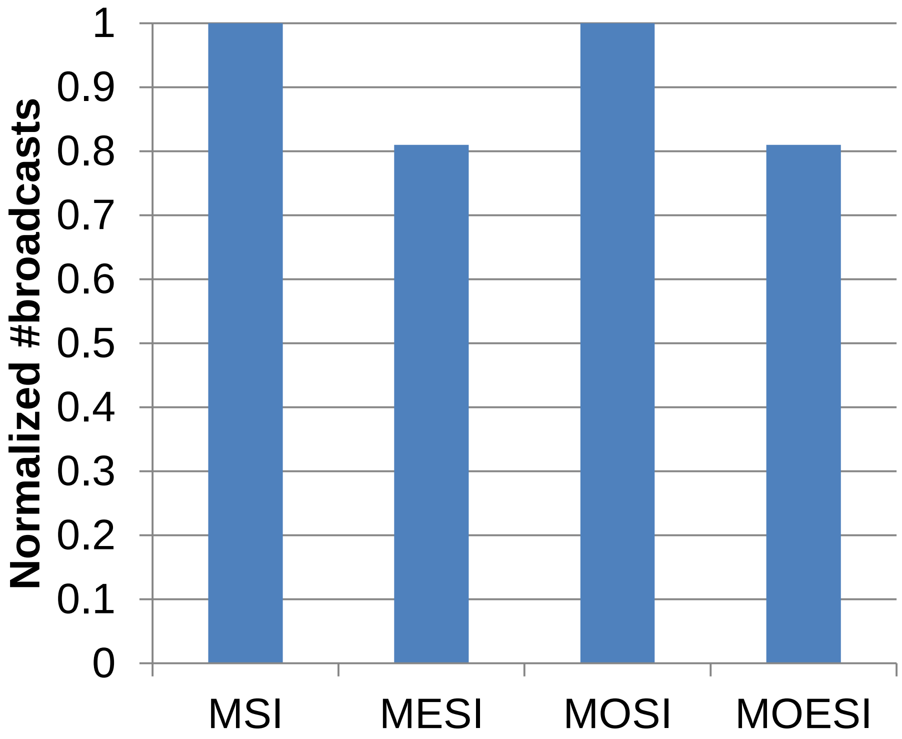
- **Benchmark = fluidanimate; input = simmedium**
- **#write-backs -11%, but leakage dominates**
- **Coherence protocol has small impact on LLC power**

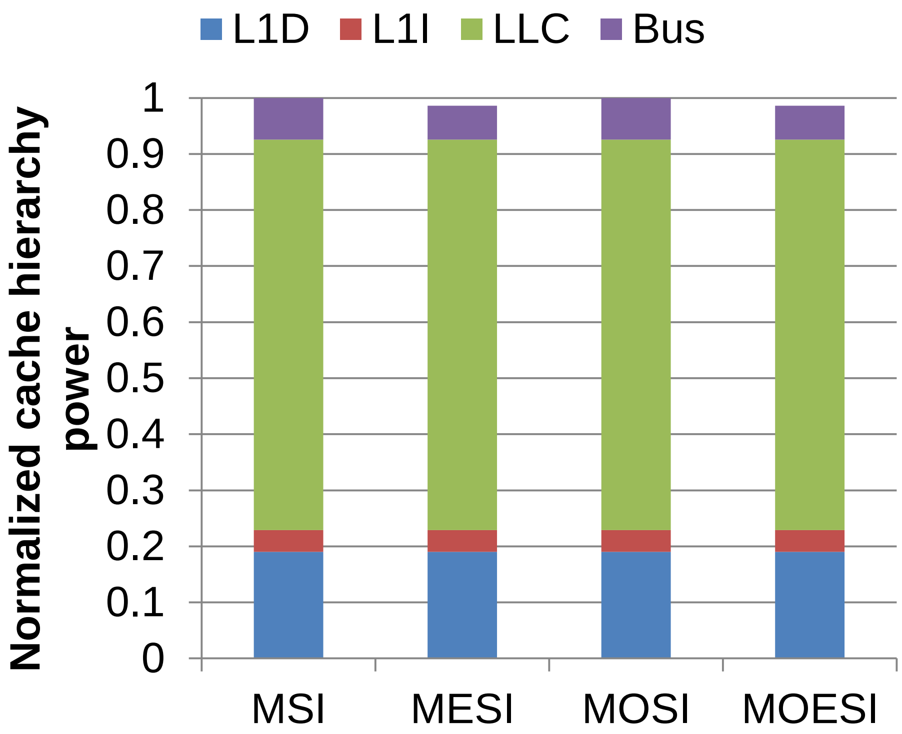
STT-RAM LLC Power



- **Benchmark = canneal; input = simmedium**
- **write-back power 43%, but #write-back almost the same**
- **Coherence protocol has small impact on LLC power**

Cache Hierarchy Power





- **Benchmark = canneal; input = simmedium**
- **#broadcasts -19%, but LLC power dominates**
- **Coherence protocol has little impact on cache hierarchy power**

Conclusion

- **Model 4 typical cache coherence protocols**
  - **MSI, MESI, MOSI, MOESI**
- **Model cache and bus power/performance**
- **Cache coherence protocol has <u>insignificant impact</u> on STT-RAM LLC power and cache hierarchy power**

Thanks

Questions?