An Extended Cell Set for Self-Timed Designs

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Abstract

it The high level synthesis approach described in [1] uses hopCP[2] language for behavioral descriptions. The behavioral specifications are then translated into Hop Flow Graphs (HFGs). The actions in the graph are then refined such that refined actions can be directly mapped onto asynchronous circuit blocks. This report describes library of such blocks called action-blocks. The action blocks use two phase transition signalling protocol for control signals and bundled protocol for data signals. The blocks have been designed using ViewLogic Design tools.
[1]

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