

A Correctness Criterion for Asynchronous Circuit Validation and Optimization

GANESH GOPALAKRISHNAN*

ERIK BRUNVAND[†]

NICK MICHELL

(ganesh@cs.utah.edu)

(brunvand@cs.utah.edu)

(michell@cs.utah.edu)

University of Utah

Dept. of Computer Science

Salt Lake City, Utah 84112

STEVEN M. NOWICK[‡]

(nowick@cs.columbia.edu)

Department of Computer Science

Room 508, Computer Science Building

Columbia University

New York, New York 10027

Keywords: Asynchronous Circuits, Circuit Optimizations, Formal Verification of Hardware, Trace Theory

Abstract. *In order to reason about the correctness of asynchronous circuit implementations and specifications, Dill has developed a variant of trace theory [1]. Trace theory describes the behavior of an asynchronous circuit by representing its possible executions as strings called "traces". A useful relation defined in this theory is called conformance, which holds when one trace specification can be safely substituted for another. We propose a new relation in the context of Dill's trace theory, called strong conformance. We show that this relation is capable of detecting certain errors in asynchronous circuits that cannot be detected through conformance. Strong conformance also helps to justify circuit optimization rules where a component is replaced by another component having extra capabilities (e.g., it can accept more inputs). The structural operators of Dill's trace theory — compose, rename and hide — are shown to be monotonic with respect to strong conformance. Experiments are presented using a modified version of Dill's trace theory verifier which implements the check for strong conformance.*