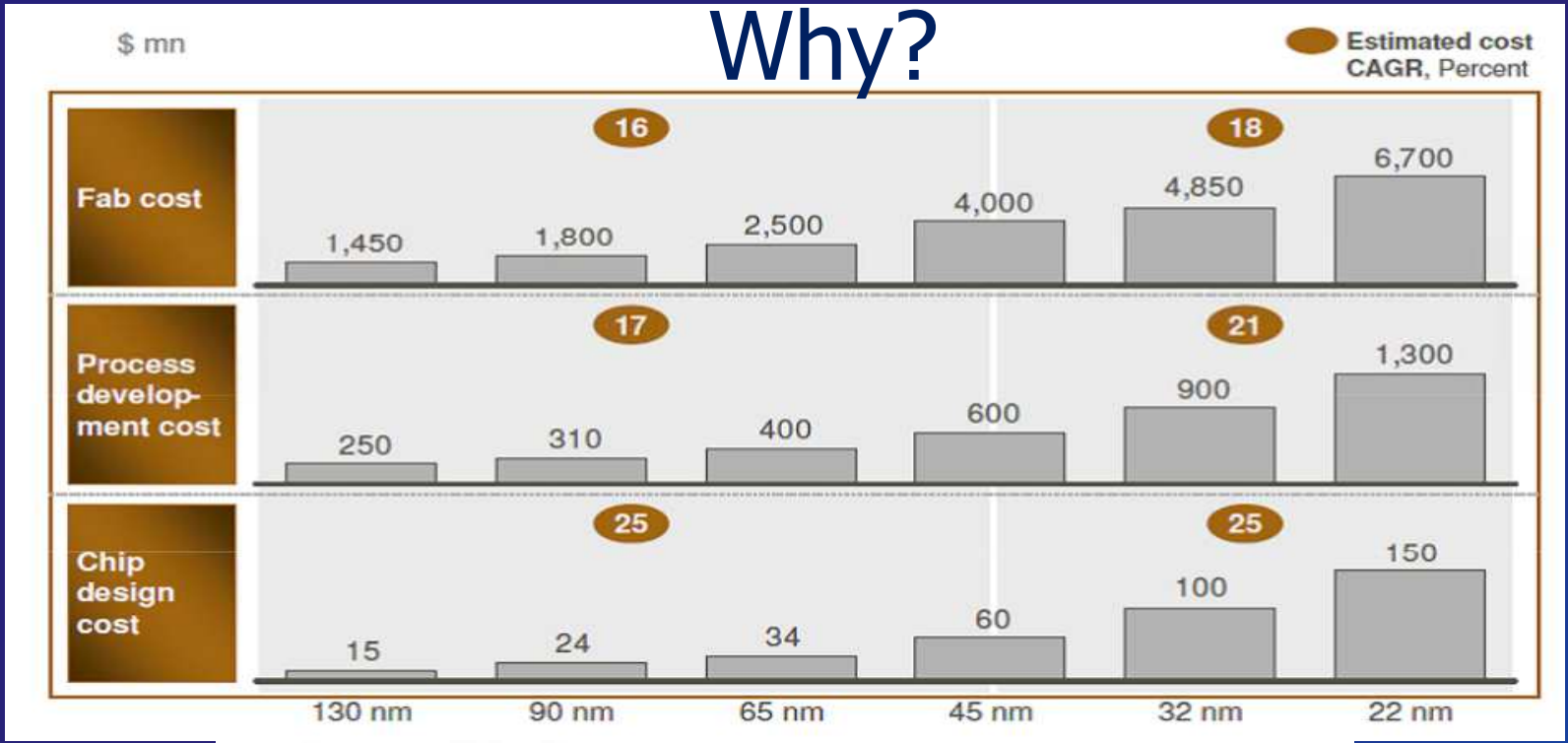
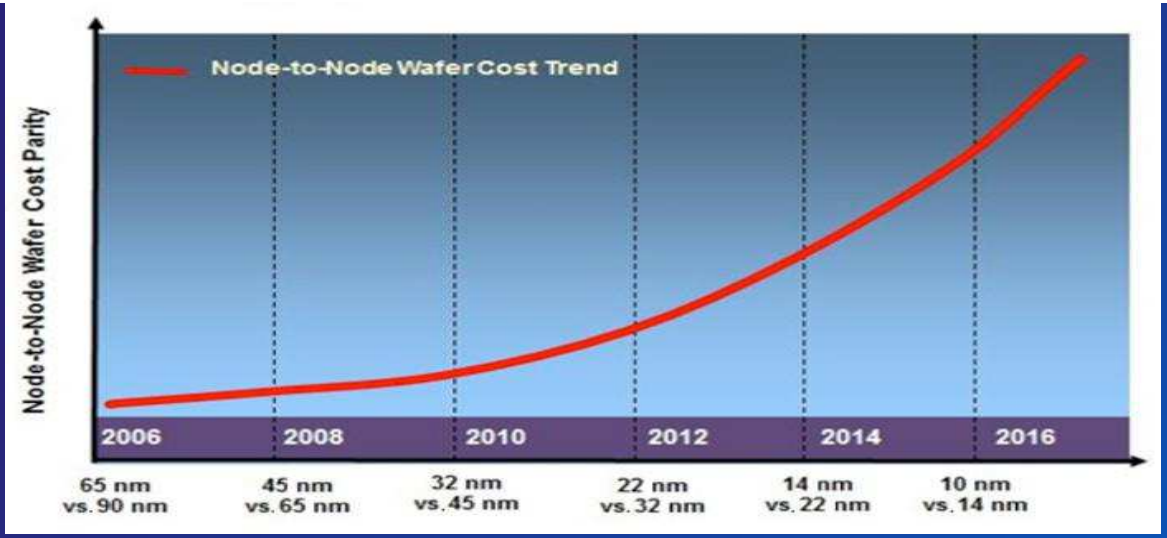
Moore's Law is Dead. Long Live Moore's Law!

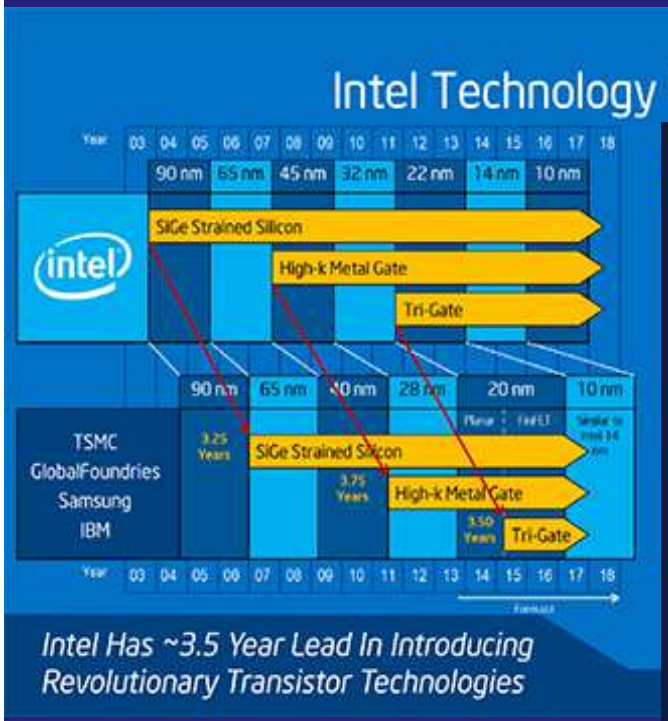
Troy Manning, Director Advanced Memory Systems

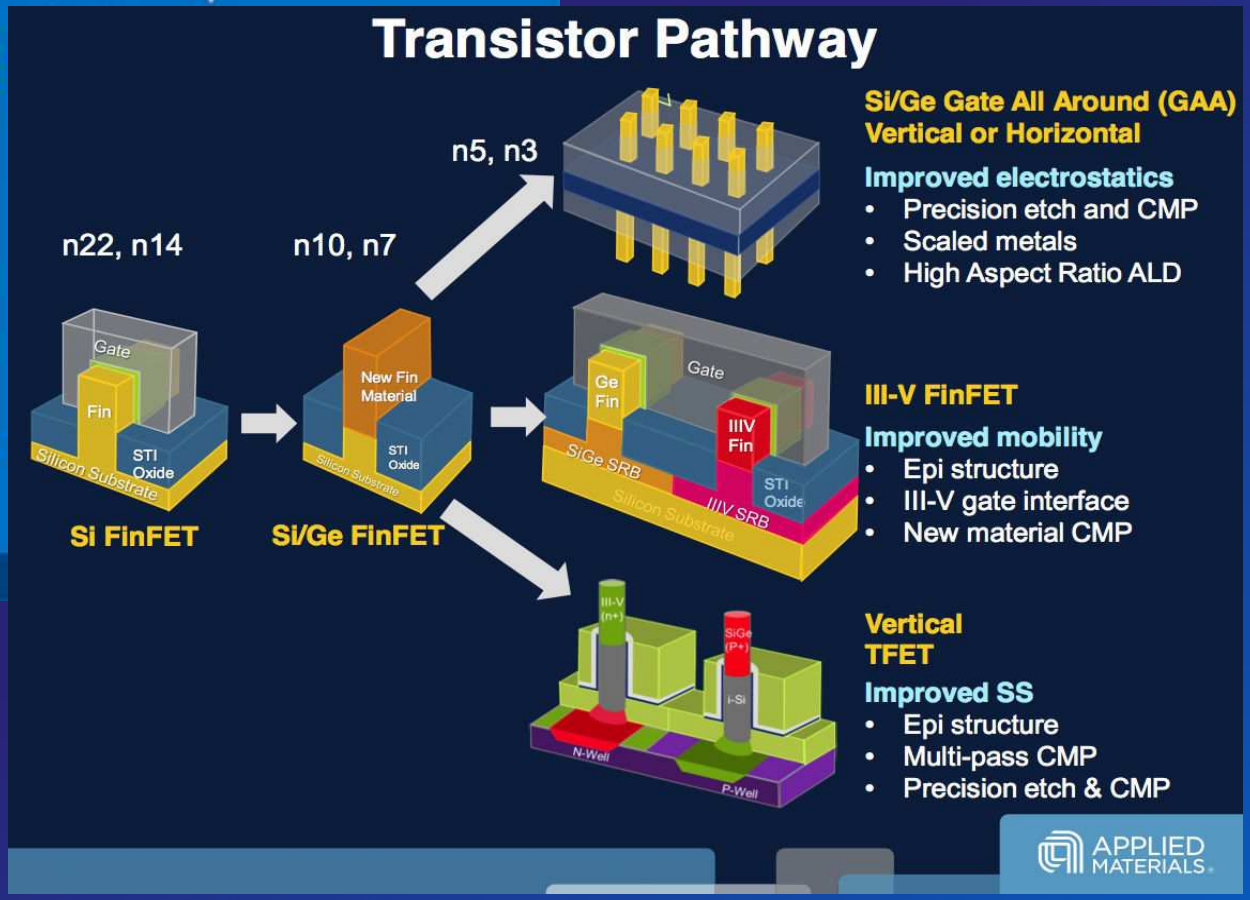
Why?


$ mn
Estimated cost CAGR, Percent
Fab cost
16
18
1,450
1,800
2,500
4,000
4,850
6,700
Process develop-ment cost
17
21
250
310
400
600
900
1,300
Chip design cost
25
25
15
24
34
60
100
150
130 nm
90 nm
65 nm
45 nm
32 nm
22 nm


Node-to-Node Wafer Cost Parity
Node-to-Node Wafer Cost Trend
2006
2008
2010
2012
2014
2016
65 nm vs. 90 nm
45 nm vs. 65 nm
32 nm vs. 45 nm
22 nm vs. 32 nm
14 nm vs. 22 nm
10 nm vs. 14 nm

Oh, the insanity!





Intel's trajectory is 5nm in 2020, 3nm 2022…then what?

Moore's Law will continue!*

- * Compute throughput and capability will continue through multidiscipline innovation, not strictly by process and transistors
- Process technology and transistor count will likely slow as expected by many
- *Fundamental computer architecture and software engineering needed!*
  - *Opportunity for Processing In or Near Memory*

Focus on Storage and Memory?

- Memory dominates the silicon area, performance, and power of the system
- Performance problems are bound by storage and memory
- Any data in storage or memory must be moved to be utilized → The "Memory Wall"
- The "Memory Wall" is changing…

Reducing Data Movement

- Processing near/in storage or memory and traveling threadlets have been proposed for years
- With proliferation of powerful, inexpensive CPUs and memory, the processing capability in peripherals is staggering…more than a y2k PC
  - HDD/SSD's contain multiple ARM CPUs, 1GB of DRAM
  - An Intel/Apple Thunderbolt cable contains ARM CPUs and 256MB of DRAM!

Processing data where the data lives

- Companies are investigating, inventing, and productizing some form of processing near the data
  - Convey Computer … EMU Solutions … Micron
- The Hybrid Memory Cube (HMC) Gen2 has simple atomic operations
- Micron has *several* other initiatives…

The Automata Processor

Video: Please link to…
http://www.youtube.com/watch?v=5guIAaOrMhk

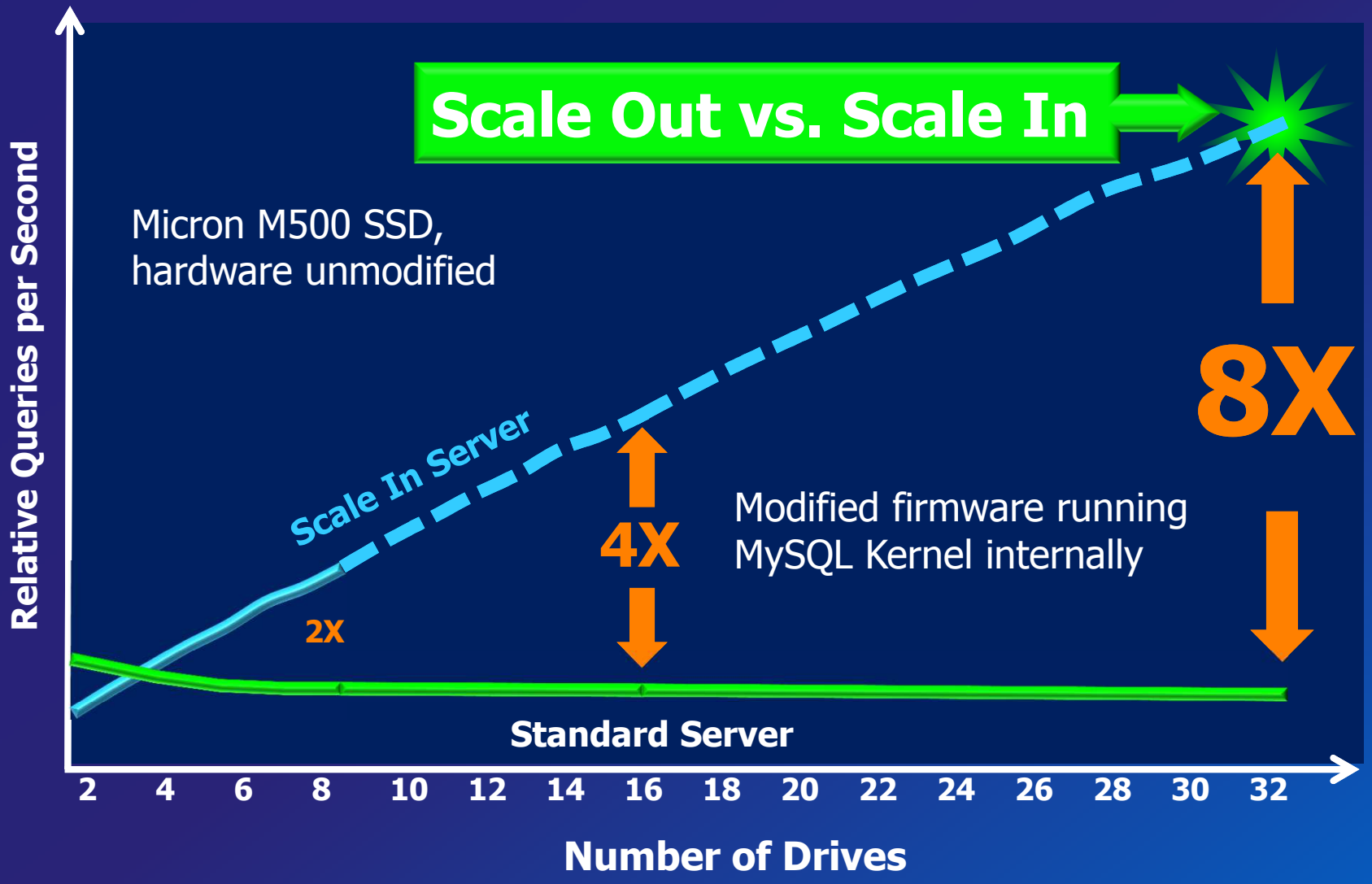
Micron

SC13 Denver 2013

The Automata Processor

- Counters and Logic elements very close to the sense amplifiers
- Massive, hierarchical compute element interconnect
- Power efficient
  - Several PJ to move a bit across a bus
  - fJ to process data near to the sense amplifiers
- Non Von Neumann…think differently!
- http://www.micron.com/automata =>tech paper

"Scale In": Processing in Storage



Source: Micron

10 concurrent search records, 40Byte Record
Server running MyISAM; Scale In Server running MyAM

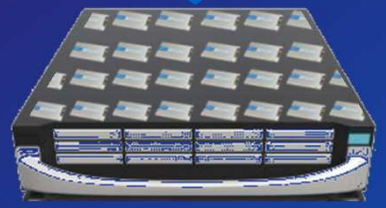
Equivalent Search Performance

Scale Out vs. Scale In

Equal Performance

8:1 Space Savings

8:1 Cost Savings



84% Power Savings

Based on 32 SSD Scale In

Deployment Challenges ~ High Rewards

- Standardized heterogeneous compute
  - Classical and embedded compute coexist transparently
  - HSA Foundation?
- Security environment
- Development pain and market inertia
  - The silicon is likely easier than the infrastructure
  - Getting the *right* silicon also challenging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